

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Venkatesh Natarajan, et al.

Serial No.: 09/451,979

Filed: October 20, 1999

For: A Method And Apparatus For Combining Memory Blocks For In Circuit Emulation



TI-28917

Art Unit: 2823

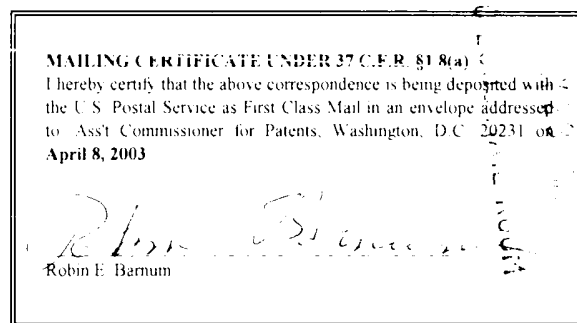
Examiner: Julio J. Maldonado

Conf. No: 4880

LETTER TO THE OFFICIAL DRAFTSPERSON

Ass't Commissioner for Patents

Washington, D.C. 20231



Sir:

Please find enclosed the formal drawings for the subject case. Charge any necessary fees to Texas Instruments Incorporated, Deposit Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

Gerald E. Laws  
Attorney for Applicant  
Reg. No. 39,268

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